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AP/ 2829

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Kazunori SAKURAI

Group Art Unit: 2829

Application No.: 09/987,409

Examiner: L. Kilday

Filed: November 14, 2001

Docket No.: 111109

For: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURE THEREOF, CIRCUIT BOARD, AND ELECTRONIC INSTRUMENT

REQUEST FOR RECONSIDERATION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In reply to the November 21, 2003 Office Action, reconsideration of the above-identified application is respectfully requested.

Claims 1-7, 17 and 18 are pending in this application.

The Office Action states that the present application may be subject to a provisional rejection under the judicially created doctrine of obviousness-type double patenting over co-pending Application No. 09/794,666, depending on the final form of the claims. However, no amendment to the claims is made. Thus, as admitted in the Office Action, no such rejection exists.

The Office Action rejects claims 1-7 under 35 U.S.C. §102(b) as being anticipated by Tsukahara, U.S. Patent No. 6,051,093. The rejection is respectfully traversed.

It is noted that claims 17 and 18 have not been listed as rejected claims under 35 U.S.C. §102(b). However, it appears that claims 17 and 18 should have been listed as

rejected claims as they are rejected in the detailed rejection on page 3 in the Office Action. Accordingly, Applicant has addressed claims 17 and 18 as also being rejected under 35 U.S.C. §102(b).

Tsukahara fails to disclose or suggest preparing a wiring substrate having a base substrate on which are formed interconnecting lines, and melting the base substrate while bumps provided on the semiconductor chip are pressed into the base substrate, as recited in claim 1 and similarly recited in claim 18.

Tsukahara merely discloses forming an external electrode terminal 33 by filling a hole 8 formed in the circuit board 4 with a conductive paste 7, positioning the external electrode terminal and a protruding bump 15 formed on an electrode of a semiconductor element 1, and pressing the semiconductor element to obtain between the conductive paste in, the hole and the protruding bumps (col. 4, lines 35-52). However, it is respectfully submitted that Tsukahara fails to disclose the process of preparing a wiring substrate having a base substrate because the circuit board 4 in Tsukahara fails to disclose a base substrate that melts while bumps provided on the semiconductor chip pressed into the substrate. In other words, the circuit board in Tsukahara is a substrate(s) that is surrounded by a copper foil 5 (Fig. 1), and does not disclose or mention melting the circuit board, as disclosed in Applicants' invention.

Further, the Office Action alleges that col. 8, lines 40-65 in Tsukahara discloses the step of melting the base substrate, while bumps provided on the semiconductor chip are pressed. Such is incorrect. The only mention of a melting process in Tsukahara is an adhesive sheet 21 that is melted and which is made of a thermosetting resin. The adhesive sheet 21 is disposed on the circuit board and the bumps on the semiconductor element are pressed through the adhesive sheet to contact the paste. At that time, the adhesive sheet 21 is melted and cured to further increase the reliability of the connection between the semiconductor electrode and the circuit board (col. 8, lines 59-60).

Accordingly, the adhesive sheet is not part of the wiring substrate that includes a base substrate to form interconnecting lines, but rather disposed on the circuit board. In other words, although Tsukahara discloses melting the adhesive sheet, the adhesive sheet is not formed with interconnecting lines because the circuit board is surrounded by the copper foil. By preparing a wiring substrate with the base substrate on which are formed interconnecting lines has significant advantages. For example, because the bumps and the connected portions of the interconnecting lines are sealed with the melted material of the base substrate, the semiconductor device can be formed from a single step and the entire device can be made thinner. Further, the stress applied to the semiconductor chip can be absorbed by the base substrate, as described in Applicant's disclosure on page 7, lines 11-16.

Further, Applicant's base substrate functions by adhering and forming interconnecting lines. By having these functions, the adhesive layer (e.g., underfill) between the semiconductor chip and the circuit board, as taught in Tsukahara, can be omitted. That is, Tsukahara discloses the step of disposing the adhesive sheet on the circuit board, whereas Applicant's invention does not require this step. Thus, it is respectfully submitted that the system and method of Tsukahara is completely different from the claimed invention.

Accordingly, Tsukahara fails to disclose or suggest preparing a wiring substrate having a base substrate upon which are formed interconnecting lines, and melting the base substrate while bumps provided on the semiconductor chip are pressed into the base substrate, as recited in claim 1, and similarly recited in claim 18.

Because Tsukahara does not literally disclose the claimed invention, it can not provide the basis for rejection under 35 U.S.C. §102. Thus, it is respectfully requested that the rejection be withdrawn.

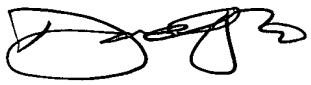
For at least these reasons, Applicant respectfully submits that Tsukahara fails to disclose the features recited in independent claims 1 and 18. Claims 2-7 and 17, which

depend from independent claim 1 are likewise distinguished over the applied art for at least the reasons discussed, as well as for the additional features they recite. Reconsideration withdrawal of the rejection are respectfully requested.

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,



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Date: February 20, 2004

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